## **REMARKS**

This is in response to the Office Action dated June 2, 2005. Claims 1-27 are pending.

Claim 1 stands rejected under 35 U.S.C. Section 102(e) as being allegedly anticipated by

Fukata (US 6,518,081). This Section 102(e) rejection is respectfully traversed for at least the following reasons.

Claim 1 as amended requires "a side light shielding layer for covering at least a portion of a side surface of the thin film transistor and side surfaces of first, second and third interlayer insulating layers, wherein the side light shielding layer is substantially vertically oriented, wherein a top surface of a dummy insulating layer is substantially at the same level as a top surface of the third interlayer insulating layer with a fourth interlayer insulating layer provided between the dummy insulating layer and the side light shielding layer." For example and without limitation, Fig. 3 of the instant application illustrates a side light shielding layer(s) (23) for covering at least a portion of a side surface of the thin film transistor and side surfaces of first (17), second (19) and third (21) interlayer insulating layers, wherein the side light shielding layer(s) (23) is substantially vertically oriented. Also, for example and without limitation, Fig. 3 of the instant application illustrates that a top surface of a dummy insulating layer (24) is substantially at the same level as a top surface of the third interlayer insulating layer (21) with a fourth interlayer insulating layer (25) provided between the dummy insulating layer (24) and the side light shielding layer (23). See also for example the instant specification at page 39, line 9 to page 40, line 22. This is advantageous, for example and without limitation, in that light may be prevented (or reduced) from being obliquely and/or laterally incident on the TFT with certainty; as a result, the light leak current of the TFT can be significantly reduced (e.g., pg. 133, lines 9-18).

Fukata fails to disclose or suggest the aforesaid underlined features of claim 1. Fukata discloses a TFT-based pixel structure including dummy contact hole 7, back shield film 3, insulating films 4, 6, 9 and 11, black matrix 12, and LDD region 15. Gate line material within the dummy contact hole 7 can block incident light from the edge of the black matrix 12 and reflected light from the edge of the back shield film 3 in the LDD region 15. However, Fukata fails to disclose or suggest a top surface of a dummy insulating layer is substantially at the same level as a top surface of the third interlayer insulating layer with a fourth interlayer insulating layer provided between the dummy insulating layer and the side light shielding layer as required by claim 1. Fukata is entirely unrelated to the invention of claim 1 in these respects.

Claim 19 requires "forming a top surface of a dummy insulating layer at substantially the same level as a top surface of the third interlayer insulating layer with a fourth interlayer insulating layer formed between the dummy insulating layer and the side light shielding layer."

Fukata fails to disclose or suggest these underlined features of claim 19.

Claim 25 requires "a top surface of a dummy insulating layer is substantially at the same level as a top surface of the third interlayer insulating film, with a fourth interlayer insulating film provided between the dummy insulating layer and the side light shielding film." Again, Fukata fails to disclose or suggest these features of claim 25.

Claim 27 requires "an insulating film provided over the thin film transistor, said insulating film having at least one hole defined therein; and a side light shielding layer for covering at least a portion of a side surface of the thin film transistor and being located on at least a sidewall of said hole in the insulating film, wherein the side light shielding layer is substantially vertically oriented, and wherein the side light shielding layer is located in said hole in the insulating film that is provided *over* the thin film transistor, and wherein no portion of the

UEDA et al Appl. No. 10/614,243

side light shielding film is located in any hole defined in an insulating film that is not formed over the thin film transistor." Fukata fails to disclose or suggest these underlined features of claim 27.

It is respectfully requested that all rejections be withdrawn. All claims are in condition for allowance. If any minor matter remains to be resolved, the Examiner is invited to telephone the undersigned with regard to the same.

Respectfully submitted,

NIXON & VANDERHYE P.C.

By:

Joseph A. Rhoa Reg. No. 37,515

JAR:caj 901 North Glebe Road, 11th Floor Arlington, VA 22203-1808

Telephone: (703) 816-4000 Facsimile: (703) 816-4100